AMENDMENTS TO THE CLAIMS:

Please amend claims 37 and 41, as shown below.

This listing of claims will replace all prior versions and listings of claims in the Application:

Claim 1 (withdrawn): A semiconductor device comprising:

active areas where transistors are formed; and

a field area for isolating said active areas from each other, said field area having a plurality of dummy areas where dummy gates are formed.

Claim 2 (withdrawn): The device as set forth in claim 1, wherein each of said dummy areas is partitioned by a shallow trench isolation layer.

Claim 3 (withdrawn): The device as set forth in claim 1, wherein each of said dummy gates has a reduced pattern of a respective one of said dummy areas.

Claim 4 (withdrawn): The device as set forth in claim 1, wherein said dummy areas and said dummy gates are square.

Claim 5 (withdrawn): The device as set forth in claim 1, wherein said dummy areas and said dummy gates are rectangular.

Claim 6 (withdrawn): The device as set forth in claim 1, wherein said dummy areas and said dummy gates are polygonal.

Claim 7 (withdrawn): The device as set forth in claim 1, wherein said dummy areas and said dummy gates are circular.

Claim 8 (withdrawn): The device as set forth in claim 1, wherein said dummy areas are arranged in rows and columns.

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Claim 9 (withdrawn): The device as set forth in claim 8, wherein the rows of said dummy areas are shifted from each other.

Claim 10 (withdrawn): The device as set forth in claim 8, wherein the columns of said dummy areas are shifted from each other.

Claim 11 (withdrawn): The device as set forth in claim 8, wherein the rows and columns of said dummy areas are shifted from each other.

Claims 12-36 (cancelled)

Claim 37 (currently amended): A method for manufacturing a semiconductor device, comprising the steps of:

forming a first photoresist pattern layer using a first photomask having active area patterns corresponding to active areas and dummy area patterns corresponding to dummy areas on a semiconductor substrate;

forming a trench in said semiconductor substrate, which trench partitions said dummy area patterns from said active area patterns, by an etching process using said first photoresist pattern layer;

forming a conductive layer over said semiconductor substrate;

forming a second photoresist pattern layer on said conductive layer using a second photomask having gate patterns corresponding to said active areas and dummy gate patterns corresponding to said dummy areas; and

patterning said conductive layer by an etching process using said second photoresist pattern layer, each of said dummy gate patterns being a reduction of a corresponding one of said dummy area patterns.

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Claim 38 (previously presented): The method as claimed in claim 37, wherein the shape of at least one said dummy area patterns and/or dummy gate patterns is a circle.

Claim 39 (previously presented): The method as claimed in claim 37, wherein a plurality of said dummy area patterns and/or dummy gate patterns are arranged in at least two rows and/or two columns.

Claim 40 (previously presented): The method as claimed in claim 39, wherein at least one said row is shifted from another said row and/or at least one column is shifted from another said column.

Claim 41 (currently amended): A method for manufacturing a semiconductor device, comprising the steps of:

forming a plurality of dummy active areas on a semiconductor substrate by using a first mask; ~~and~~

forming a trench in said substrate, which trench partitions said dummy active areas from active areas by an etching process using said first mask; and

forming a plurality of dummy gates on said dummy active areas by using a second mask corresponding to said first mask.

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